Experimental Tests of DC SFCL under Low Impedance and High Impedance Fault Conditions

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***Abstract*—DC system protection is more challenging than that for AC system due to the rapid rate of rise of the fault current and absence of natural current zero-crossing in DC systems. Superconducting fault current limiter (SFCL) in DC systems is a promising technology to reduce the fault current level and the rate of rise of the fault current, and also SFCLs have no resistance during normal operation. In this paper, the behaviors of an SFCL coil are investigated under both low impedance and high impedance fault conditions in DC systems. In the low impedance fault condition system, the SFCL coil performs effective limitation of the fault current level under different prospective fault current levels. The application of SFCLs with limited inductance in the DC system can be a potential solution to effectively suppress the fault current under low impedance short-circuit faults. The SFCL coil under the high impedance fault condition can only limit the prospective fault current when it is much higher than the critical current of the coil.**

***Index Terms*—Fault current limiters, power system protection, short-circuit currents, yttrium barium copper oxide (YBCO).**

I. Introduction

DC systems have many advantages over AC systems including lower power loss, higher efficiency, better controllability and higher reliability [1]. Many voltage source converter (VSC) based medium voltage direct current (MVDC) distribution system projects have been carried out all over the world, such as RWTH Aachen University MVDC grid in Germany [2] and the Tangjia Bay pilot project in China [3], [4]. However, due to the fast discharge of the DC capacitors and the low impedance in DC systems, the fault current can increase to more than tens of times the rated current in a few milliseconds [5]. The fault current limitation and fault current interruption are two main technical challenges for the DC system protection.

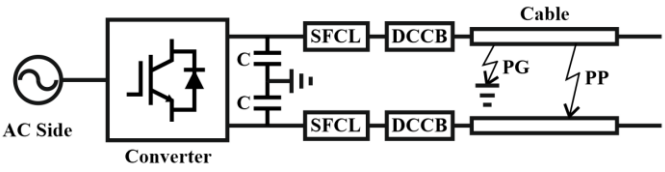

Fig. 1. Protection devices and typical fault types in DC systems

Fig. 1 illustrates protection devices in a typical structure of a DC system. Superconducting fault current limiters (SFCLs) and DC circuit breakers (DCCBs) are the main protection devices to protect the DC system against any potential high fault current. Many DCCBs have been successfully developed to isolate the fault current in several milliseconds [6]–[10]. GEIRI has developed a ± 200 kV hybrid DCCB for the Zhoushan five-terminal HVDC project, which can break 15 kA within 3 ms [8]. NR Electric Co., Ltd. and GEIRI have built ± 535 kV hybrid DCCBs for the Zhangbei four-terminal HVDC project, which can interrupt 25 kA within 3 ms [9], [10]. Resistive SFCLs are promising candidates to reduce fault currents to acceptable levels in DC systems allowing DC circuit breakers to operate quickly and reliably [11], [12], because of the simplicity, compactness and little impact on the power system. Superconducting material can exhibit zero resistance in the superconducting state, and show a finite resistance once quenched [13]. A 20 kV/400 A noninductive type resistive SFCL bases on yttrium barium copper oxide (YBCO) conductors was developed for ± 10 kV VSC-based DC system at Suzhou Nami substation, which consists of 8 solenoid coils in series and successfully passed the test to limit a prospective fault current of 8 kA to 2.26 kA in 2019 [14]. A 160 kV/1 kA DC resistive SFCL based on rare earth barium copper oxide (REBCO) tape has been developed and installed at the Nan'ao ±160 kV HVDC power grid in China, which is the highest voltage level and the largest capacity in the world so far. This SFCL consists of 24 pancake coils with noninductive winding [15], [16]. In the European Union FASTGRID project, a 50 kV/1.5 kA DC resistive SFCL module will be developed and tested. The module will be comprised of 10 bifilar pancake coils using REBCO tapes [17].

In AC systems, the inductance of a resistive SFCL should be minimized to reduce AC losses and the voltage drop during normal operation [18]. However, a resistive SFCL for DC sys-

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tems can exist an inductance because there is no voltage drop in the steady state [19]. So it is not crucial to design a resistive SFCL with low-inductive or non-inductive characteristics for DC systems. The impact of the resistive SFCL with certain inductance needs to be evaluated in DC systems.

There are two common short-circuit fault types in DC systems, pole-to-ground (PG) faults and pole-to-pole (PP) faults, as shown in Fig. 1. The pole-to-ground faults are the most likely short-circuit faults in DC systems, which are mainly caused by insulation degradation. The pole-to-ground faults can be either low impedance faults or high impedance faults depending on the grounding impedance. The pole-to-pole faults are generally low impedance faults [20]. Under the low impedance faults, the fault current can be higher than tens of times of normal operating current. Under the high impedance faults, the fault current is not sufficient to trip the overcurrent relays due to high grounding impedance [21]. In this paper, the behaviors of a resistive SFCL under the low impedance fault and high impedance fault are investigated.

II. DC Fault Current Response Analysis

In VSC-based DC systems, different stages of the fault current response have been defined and studied, including capacitor discharge stage (natural response) in the DC side, diode freewheel stage (natural response) in the converter side, and grid-side current feeding stage (forced response) in the AC side [22]. During the capacitor discharge stage, the fault current amplitude can reach more than tens of times the rated current value [5], [23]. Considering the influence and the severity of the fault current, the capacitor discharge stage is analyzed in this section.

When a short-circuit fault occurs, the DC link capacitor close to the output of the converter discharges through the fault current loop leading to a large DC fault current, as shown in Fig. 2.

In the Laplace domain, the current response of the second-order *RLC* equivalent circuit can be expressed as:

$$I(s)=\frac{u_c(0\_)+sLi(0\_)}{s^2L+sR+\frac{1}{C}} \tag{1}$$

where $u_c(0\_)$ and $i_L(0\_)$ are the voltage level across the capacitor and current flowing through the inductor before the fault occurs. R represents the total resistance of the short-circuit loop, including the line resistance and the fault resistance. L represents the total inductance of the short-circuit loop. C is the capacitance of the DC link capacitor.

The roots of the polynomial in the denominator of the Laplace equation are derived as follows:

$$s_{1,2}=-\delta\pm\sqrt{\delta^2-\omega_0^2} \tag{2}$$

where δ and ω_0 are the damping factor and resonant angular frequency, respectively, which are defined as:

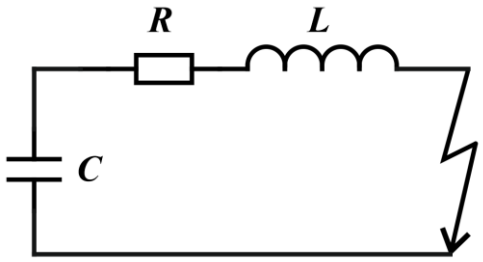

Fig. 2. *RLC* equivalent circuit during the capacitor discharge stage

$$\delta=\frac{R}{2L} \tag{3}$$

$$\omega_0=\frac{1}{\sqrt{LC}} \tag{4}$$

According to the relationship between δ^2 and ω_0^2, the *RLC* system can be classified into three types: overdamped, critically damped, and underdamped.

$$\text{if}\quad \delta^2-\omega_0^2,\begin{cases}>0, & \text{overdamped}\\ =0, & \text{critically damped}\\ <0, & \text{underdamped}\end{cases} \tag{5}$$

In terms of fault currents, the short-circuit faults with the underdamped system are the crucial situations to be analyzed. In the underdamped system ($R<2\sqrt{L/C}$), s_1 and s_2 are two complex roots. The voltage u_c oscillated, and it will be less than zero. Because the DC link capacitor dominates the fault current during the discharge stage and the initial current through the inductor is relatively low, the fault current response in the underdamped oscillation can be simplified as

$$i(t)=\frac{u_c(0\_)}{\omega L}e^{-\delta t}\sin(\omega t) \tag{6}$$

where ω is the damped resonant frequency, which is given by

$$\omega=\sqrt{\omega_0^2-\delta^2} \tag{7}$$

So, when the derivative of the fault current response in (6) reaches zero, t_{peak} for the fault current to reach its peak amplitude can be obtained. For the highly underdamped system, where $\omega\approx\omega_0$, the time t_{peak} can be expressed as

$$\begin{aligned}t_{peak}&=\frac{1}{\omega_0}\arctan\frac{\omega_0}{\delta}\\&=\sqrt{LC}\arctan\left(\frac{2}{R}\sqrt{\frac{L}{C}}\right)\end{aligned} \tag{8}$$

According to (3), (6) and (8), increasing the loop resistance R can reduce peak fault current and increasing the loop inductance L can postpone the fault current to reach the peak value in the highly underdamped system, both methods will reduce the requirement of the DC circuit breaker.

III. Experimental Setup

A. SFCL Coil

A 12 mm wide YBCO tape manufactured by Shanghai Superconductor Technology Co., Ltd. (SHSC) is used for the resistive SFCL coil design. The specifications of the SFCL coil are listed in Table I. As shown in Fig. 3, the SFCL coil has 10 turns of the YBCO tape wound onto a PTFE tube with a diameter of 90 mm, the total length of the tape is 3 m. Two voltage taps are soldered close to both ends of the coil to measure the voltage drop across the SFCL coil, and the distance between two voltage taps along the wire is 2.74 m. The inductance and resistance of the SFCL coil at room temperature are 5.3 μH and 350 mΩ. The critical current of the SFCL coil is measured to be 267 A at 77 K.

B. Platform

The natural response of the SFCL coil was tested using an inductor-capacitor (LC) resonant circuit, which can emulate the rising of the fault current of the DC system. The schematic diagram of the DC fault current test circuit is presented in Fig. 4. The capacitance is 12 mF, and two air core inductors are designed to represent different system fault conditions: a 23 μH inductor to simulate low impedance fault and a 1 mH inductor to simulate high impedance fault, respectively. The SFCL coil, immersed in liquid nitrogen (LN_2) bath, is connected in series with the inductor. The switch is turned off after the capacitor is charged to the desired level by a DC power supply. Once the thyristor is triggered, the fault current flows through the SFCL coil. The diode represents the freewheeling diodes in the converter side and it can protect the capacitor from any possible high reverse voltage. The system parameters under two fault conditions are listed in Table II, and the system before inserting the SFCL coil in the capacitor discharge stage is underdamped.

IV. Experimental Results and Discussion

A. Experimental Results under Low Impedance Fault

The 23 μH inductor is connected to the test platform during the tests to represent the fault with low impedance. The experiments were carried out under the prospective fault currents from 162 A to 1042 A. Experimental results with two prospective fault currents (314 A and 1042 A) are presented in Fig. 5. The solid line denotes the prospective fault current without the SFCL coil, and the dotted line shows the current with the SFCL coil. The long-dashed line is the voltage drop across the SFCL coil measured between the two voltage taps.

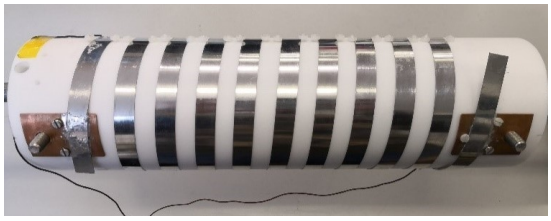

Fig. 3. SFCL coil prototype

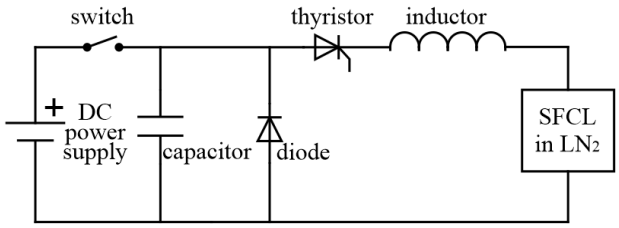

Fig. 4. Schematic diagram of DC fault test circuit

In Fig. 5 (a), the peak fault current is reduced from 314 A to 276 A when the SFCL coil is connected to the circuit due to the presence of the inductance of the SFCL coil. In addition, t_{peak} increases from 0.8 ms to about 0.9 ms after introducing the SFCL coil, which is consistent with the results calculated using (8). In Fig. 5 (b), the peak fault current is reduced from 1042 A to 680 A with the SFCL coil, which is limited by both inductance and quench resistance of the SFCL coil. The increased resistance in the fault current loop has a greater impact on t_{peak} than the increased inductance, so the peak time reduces from 0.8 ms to around 0.7 ms.

It should be pointed out that there is a voltage spike across the SFCL at the beginning of the fault, which is induced by the inductance of the SFCL coil. Therefore, the inductance of an SFCL coil should be carefully designed in case any voltage across the SFCL coil is higher than the insulation voltage level of the cryostat system. In Fig. 5 (b), there is a second voltage peak, which is caused by the quench of the SFCL coil. The voltage starts to increase when the fault current is higher than the critical current of the SFCL coil and reaches the peak value near the peak current level.

TABLE I
Specification of SFCL coil

Parameter	Value
Tape manufacturer	SHSC
Superconducting layer	YBCO
Tape width	12 mm
Tape length	3 m
Tube material	PTFE
Tube diameter	90 mm
Coil turn number	10
Coil pitch length	24 mm
Distance between voltage taps	2.74 m
Coil inductance @ room temperature	5.3 μH
Coil resistance @ room temperature	350 mΩ
Coil critical current @ 77 K	267 A

TABLE II
System conditions before inserting the SFCL coil

Parameter	Low impedance fault	High impedance fault
Loop inductance, L	23 μH	1 mH
Loop resistance, R	5 mΩ	61 mΩ
Capacitance, C	12 mF	12 mF
Damping factor, δ	108.7	30.5
Resonant angular frequency, ω_0	1903.5	288.7
System condition	Underdamped	Underdamped

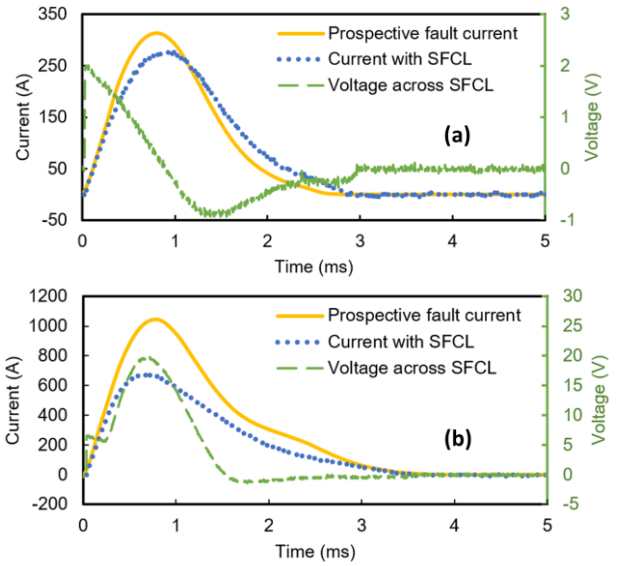

Fig. 5. Experimental results under low impedance fault condition: (a) 314 A prospective fault current; (b) 1042 A prospective fault current

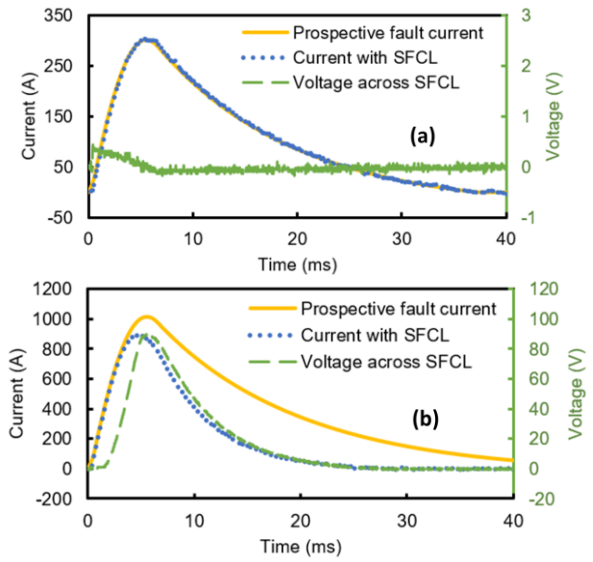

Fig. 6. Experimental results under high impedance fault condition: (a) 302 A prospective fault current; (b) 1017 A prospective fault current.

B. Experimental Results under High Impedance Fault

The 1 mH inductor is connected to the test platform during the tests to represent the fault with high impedance. Experimental results with two prospective fault currents (302 A and 1017 A) under the high impedance fault condition are presented in Fig. 6.

In Fig. 6 (a), there is almost no current reduction with the SFCL coil although the prospective current is 13% higher than the critical current. In Fig. 6 (b), the prospective current is almost four times as high as the critical current, and the peak fault current is reduced from over 1 kA to 880 A when using the SFCL coil. This means the prospective current is limited to 86.5% by the SFCL coil. The voltage drop across the SFCL coil starts to increase when the current is higher than the critical current. Under the high impedance fault, the fault current is relatively low and even not sufficient to trip the overcurrent relay. It is expected that SFCL does not have an effective current limitation under this condition as the fault current level is low.

C. Comparison under Two Fault Conditions

Fig. 7 shows the current limiting performance and the maximum quench resistance of the SFCL coil under various normalized prospective currents under two fault conditions. For both fault conditions, the SFCL coil performs better current limitation capability as the prospective fault current increases.

Under the low impedance fault condition, the inductance of the SFCL coil has an obvious influence on the current limitation. As shown in Fig. 7, when the prospective current is lower than the critical current of the SFCL coil, the peak current is still limited to 89% by the SFCL coil. When the prospective fault current is about four times higher than the critical current, the peak value of the prospective fault current is limited to 65% by the SFCL coil and the peak quench resistance of the SFCL coil is about 30 mΩ, which is only 8.6% of the resistance at room temperature. Therefore, the SFCL coil with

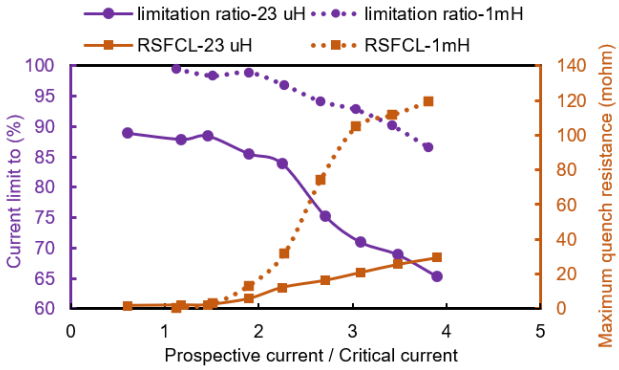

Fig. 7. Current limitation with the SFCL and maximum quench resistance (RSFCL) as a function of the prospective current (normalized). The low impedance fault condition uses the 23 μH inductor and the high impedance fault condition uses the 1 mH inductor.

inductance can effectively suppress the fault current rate of rise and reduce the peak fault current level for a low impedance fault condition.

However, the SFCL coil starts to exhibit the current limiting performance under the high impedance fault condition until the prospective peak current is close to twice the critical current. As the prospective current increases to four times the critical current, the prospective fault current is limited to 86.5% and the maximum quench resistance reaches 119 mΩ. This resistance value is about one-third of the resistance measured at room temperature. So the resistance of the SFCL coil dominates the current limiting performance for the high impedance fault condition.

Although the quench resistance under the low impedance fault condition is only about one-fourth of that under the high impedance fault condition when the fault current is close to four times the critical current, the effectiveness of the SFCL coil under the low impedance fault condition is better. The in-

ductance of the SFCL coil under low impedance fault condition has a significant impact on the current limitation, and it can always suppress the fault current rate of rise and reduce the peak fault current level. Therefore, to limit the fault current for DC systems with the low impedance fault loop, such as electric aircraft and electric ships, a resistive SFCL coil with the inductance characteristic can be considered.

V. Conclusion

The inductance of the resistive SFCL coil dominates the fault current under the low impedance fault condition, whereas the resistance dominates the fault current under the high impedance fault condition.

The SFCL coil has an effective current limiting performance under the low impedance fault condition in the DC system, even if the prospective fault current is lower than the critical current of the SFCL coil. Both the rising rate of fault current and the peak fault current level can be limited by the SFCL coil when the coil inductance is comparable with the fault loop inductance. Therefore, SFCLs with finite inductances, which provide the same magnitude of impedance with the system impedance during the fault, are promising candidates to limit the fault current under the low impedance short-circuit fault in DC systems.

References

[1] F. Wang, Y. Pei, D. Boroyevich, R. Burgos, and K. Ngo, "AC vs. DC distribution for off-shore power delivery," in *2008 34th Annual Conference of IEEE Industrial Electronics*, 2008, pp. 2113-2118: IEEE.

[2] F. Mura and R. W. De Doncker, "Design aspects of a medium-voltage direct current (MVDC) grid for a university campus," in *8th International Conference on Power Electronics-ECCE Asia*, 2011, pp. 2359-2366: IEEE.

[3] L. Qu et al., "Planning and analysis of the demonstration project of the MVDC distribution network in Zhuhai," *Frontiers in Energy*, vol. 13, no. 1, pp. 120-130, 2019.

[4] W. Li et al., "State of the art of researches and applications of MVDC distribution systems in power grid," in *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, 2019, vol. 1, pp. 5680-5685: IEEE.

[5] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC microgrid protection: a comprehensive review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[6] M. Callavik, A. Blomberg, J. Häfner, and B. Jacobson, "The hybrid HVDC breaker," *ABB Grid Systems Technical Paper*, vol. 361, pp. 143-152, 2012.

[7] X. Pei, O. Cwikowski, D. Vilchis-Rodriguez, M. Barnes, A. Smith, and R. Shuttleworth, "A review of technologies for MVDC circuit breakers," in *Industrial Electronics Society, IECON 2016-42nd Annual Conference of the IEEE*, 2016, pp. 3799-3805: IEEE.

[8] W. Zhou et al., "Development and test of a 200kV full-bridge based hybrid HVDC breaker," in *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, 2015, pp. 1-7: IEEE.

[9] B. Yang, D. Cao, W. Shi, W. Lv, W. Wang, and B. Liu, "A novel commutation-based hybrid HVDC circuit breaker," in *CIGRE Winnipeg Colloquium*, pp. A3-15, 2017.

[10] G. Tang, H. Pang, Z. He, and X. Wei, "Research on key technology and equipment for Zhangbei 500kV DC grid," in *2018 International Power Electronics Conference (IPEC-Niigata 2018-ECCE Asia)*, 2018, pp. 2343-2351: IEEE

[11] X. Pei, A. C. Smith, and M. Barnes, "Superconducting fault current limiters for HVDC systems," *Energy Procedia*, vol. 80, pp. 47-55, 2015.

[12] B. Xiang, Z. Liu, C. Wang, Z. Nan, Y. Geng, J. Wang, and S. Yanabu, "DC interrupting with self-excited oscillation based on superconducting current-limiting technology," *IEEE Transactions on Power Delivery*, pp. 529-536, vol. 33, no. 1, Feb. 2018.

[13] M. Yazdani-Asrami, M. Staines, G. Sidorov, M. Davies, J. Bailey, N. Allpress, and S. A. Gholamian, "Fault current limiting HTS transformer with extended fault withstand time," *Superconductor Science and Technology*, vol. 32, no. 3, p. 035006, 2019.

[14] J. Sun et al., "Design and performance test of a 20-kV DC superconducting fault current limiter," *IEEE Transactions on Applied Superconductivity*, vol. 30, no. 2, pp. 1-5, 2020.

[15] M. Song et al., "The parameter design and system simulation of 160-kV/1-kA resistive-type superconducting DC fault current limiter," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1-6, 2019.

[16] B. Li et al., "RQ Curve based evaluation method for current-limiting performance of DC R-SFCL in high voltage DC system," *Superconductor Science and Technology*, 2020.

[17] P. Tixador et al., "Status of the European Union project FASTGRID," *IEEE Transactions on Applied Superconductivity*, vol. 29, no. 5, pp. 1-5, 2019.

[18] W. Song, X. Pei, J. Xi and X. Zeng, "A novel helical superconducting fault current limiter for electric propulsion aircraft," *IEEE Transactions on Transportation Electrification*, vol. 7, no. 1, pp. 276-286, 2021.

[19] P. Tixador and A. Badel, "Resistive SFCL Design," in *Superconducting Fault Current Limiter: Innovation For The Electric Grids*, vol. 3, pp. 85-115, 2018.

[20] D. Salomonsson, L. Soder, and A. Sannino, "Protection of low-voltage DC microgrids," *IEEE Transactions on Power Delivery*, vol. 24, no. 3, pp. 1045-1053, 2009.

[21] A. Ghaderi, H. L. Ginn III, and H. A. Mohammadpour, "High impedance fault detection: a review," *Electric Power Systems Research*, vol. 143, pp. 376-388, 2017.

[22] J. Yang, J. E. Fletcher, and J. O'Reilly, "Short-circuit and ground fault analyses and location in VSC-based DC network cables," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 10, pp. 3827-3837, 2011.

[23] S. Fletcher, P. Norman, S. Galloway, and G. Burt, "Determination of protection system requirements for DC unmanned aerial vehicle electrical power networks for enhanced capability and survivability," *IET Electrical Systems in Transportation*, vol. 1, no. 4, pp. 137-147, 2011.